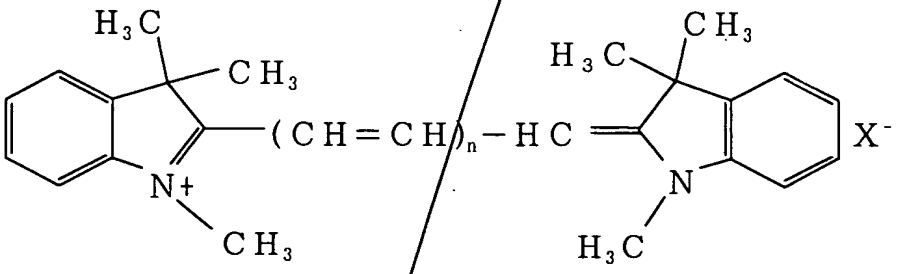
WHAT IS CLAIMED IS:

1. A copper electroplating bath comprising a solution containing copper ions and at least one of electrolytes with an addition of at least one of cyanine dyes.

2. A copper electroplating bath comprising a solution containing copper ions and at least one of electrolytes with an addition of at least one of indolium compounds.

3. A copper electroplating bath comprising a solution containing copper ions and at least one of electrolytes with an addition of at least one of the compounds represented by the following general formula (I):



(I)

where X^- is an anion, and n is 0, 1, 2, or 3.

4. The copper electroplating bath according to Claim 1, wherein one or more of polyethers, organic sulfur compounds and halide ions is further added to said copper electroplating bath.

5. The copper electroplating bath according to Claim 2, wherein one or more of polyethers, organic sulfur compounds and halide ions is further added to

said copper electroplating bath.

6. The copper electroplating bath according to Claim 3, wherein one or more of polyethers, organic sulfur compounds and halide ions is further added to said copper electroplating bath.

7. The copper electroplating bath according to Claim 1, wherein at least one or more of said cyanine dyes is added at a concentration of 1 to 15 mg/L.

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8. The copper electroplating bath according to Claim 2, wherein at least one or more of said indolium compounds is added at a concentration of 1 to 15 mg/L.

9. The copper electroplating bath according to Claim 3, wherein at least one or more of the compounds of the general formula (I) is added at a concentration of 1 to 15 mg/L.

10. A process for producing a semiconductor integrated circuit device comprising providing an insulating layer having features on the top of the major surface of a semiconductor wafer which has a plurality of circuit element areas formed, depositing a barrier metal layer and a seed metal layer on the bottoms and the side surfaces of said features and on the top surface of said insulating layer, and filling the inside of said features with copper by electroplating with the copper electroplating bath according to Claim 1.

11. A process for producing a semiconductor integrated circuit device comprising providing an

insulating layer having features on the top of the major surface of a semiconductor wafer which has a plurality of circuit element areas formed, depositing a barrier metal layer and a seed metal layer on the bottoms and the side surfaces of said features and on the top surface of said insulating layer, and filling the inside of said features with copper by electroplating with the copper electroplating bath according to Claim 2.

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12. A process for producing a semiconductor integrated circuit device comprising providing an insulating layer having features on the top of the major surface of a semiconductor wafer which has a plurality of circuit element areas formed, depositing a barrier metal layer and a seed metal layer on the bottoms and the side surfaces of said features and on the top surface of said insulating layer, and filling the inside of said features with copper by electroplating with the copper electroplating bath according to Claim 3.